



# Flash Wafer Fabrication Change and Gold (Au) To Copper (Cu) Transition for Spartan-3AN FPGA Devices

XCN14003 (v1.3) October 27, 2014

Product Change Notice

## Overview

The purpose of this notification is to communicate a change in wafer fabrication facility location and process technology (non-optical) shrink from 0.13um to 0.11um for the in-system flash memory used in the Spartan®-3AN FPGA devices. In addition, Xilinx is transitioning the wire bond packages from gold (Au) to copper (Cu) wires meeting industry trends.

## Description

Xilinx is transitioning the in-system flash memory for the Spartan-3AN FPGA devices from wafer fabrication facility X-FAB (0.13um process) to UMC (0.11um process). Xilinx is performing the qualification and characterization on the Spartan-3AN FPGA devices which include the in-system flash with 0.11um process. Form, fit, and function will not be affected with this change. Ancillary programming algorithm changes are specified in the [Xilinx Answer 59572](#).

To align with the current industry trends and Xilinx product line strategy, we will transition the Spartan-3AN FPGA family from gold (Au) to copper (Cu) wire. This change will not affect fit, form, function or MSL rating of the wire bond packages. Xilinx has successfully implemented Spartan®-3/-3E/-3A with copper wire since August 2011, please refer to [XCN11002](#). For the Cu-wire assembly, only halogen free, EU-ROHS compliant package and green mold compound will be used. The package does not contain published REACH SvHC materials.

## Products Affected

This change affects all speed, package, and temperature variations of the commercial (C) and industrial (I) grade devices. Automotive (XA) and Hi-Rel (XQ) devices are not affected by this Product Change Notice. Affected part numbers are included in the following [Table 1](#):

Table 1: Spartan-3AN FPGA Device/Package Affected

| Device                    | Package  |
|---------------------------|----------|
| XC3S50AN <sup>(2)</sup>   | TQ(G)144 |
| XC3S200AN                 | FT(G)256 |
| XC3S400AN                 | FT(G)256 |
|                           | FG(G)400 |
| XC3S700AN                 | FG(G)484 |
| XC3S1400AN <sup>(2)</sup> | FG(G)676 |

Notes:

1. Please refer to the [Xilinx Answer 59572](#) for ancillary programming algorithm changes.
2. Certain parts under XC3S50AN and XC3S1400AN devices have been discontinued; please refer to [XCN13016](#). The parts affected by XCN13016 are not affected by this Product Change Notice.

Table 2: Spartan-3AN FPGA Family Product Affected

| Part Number            | Part Number        | Part Number            | Part Number             |
|------------------------|--------------------|------------------------|-------------------------|
| XC3S50AN-4TQ144C4100   | XC3S200AN-5FT256C  | XC3S400AN-5FGG400C     | XC3S1400AN-4FG676I      |
| XC3S50AN-4TQ144I4100   | XC3S200AN-5FTG256C | XC3S400AN-5FT256C      | XC3S1400AN-4FG676I4301  |
| XC3S50AN-4TQG144C      | XC3S400AN-4FG400C  | XC3S400AN-5FTG256C     | XC3S1400AN-4FGG676C     |
| XC3S50AN-4TQG144I      | XC3S400AN-4FG400I  | XC3S700AN-4FG484C      | XC3S1400AN-4FGG676C4301 |
| XC3S50AN-5TQG144C      | XC3S400AN-4FGG400C | XC3S700AN-4FG484I      | XC3S1400AN-4FGG676I     |
| XC3S200AN-4FT256C      | XC3S400AN-4FGG400I | XC3S700AN-4FGG484C     | XC3S1400AN-4FGG676I4301 |
| XC3S200AN-4FT256I      | XC3S400AN-4FT256C  | XC3S700AN-4FGG484I     | XC3S1400AN-5FG676C      |
| XC3S200AN-4FTG256C     | XC3S400AN-4FT256I  | XC3S700AN-5FG484C      | XC3S1400AN-5FG676C4301  |
| XC3S200AN-4FTG256C0862 | XC3S400AN-4FTG256C | XC3S700AN-5FGG484C     | XC3S1400AN-5FGG676C     |
| XC3S200AN-4FTG256I     | XC3S400AN-4FTG256I | XC3S1400AN-4FG676C     | XC3S1400AN-5FGG676C4301 |
| XC3S200AN-4FTG256I0913 | XC3S400AN-5FG400C  | XC3S1400AN-4FG676C4301 |                         |

## Key Date and Cross Shipping Information

Current and new product cutover will begin as indicated in FAQ (XTP343) Table 1. Dates may be subjected to change based on customer demand and or usage.

## Qualification Data

Qualification data is available upon request.

## Response

No response is required. For additional information or questions, please contact [Xilinx Technical Support](#).

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## Additional Documentation

XTP343 - FAQ: Implications of XCN14003  
<https://secure.xilinx.com/webreg/clickthrough.do?cid=370908>.

## Revision History

The following table shows the revision history for this document:

| Date       | Version | Description of Revisions                                                                               |
|------------|---------|--------------------------------------------------------------------------------------------------------|
| 05/05/2014 | 1.0     | Initial release.                                                                                       |
| 05/26/2014 | 1.1     | (Pg. 1) Added the XC3S700AN: Impacted by the ancillary programming algorithm changes.                  |
| 10/06/2014 | 1.2     | Updated reference to Xilinx Answer 59572 for ancillary programming changes for all affected devices.   |
| 10/27/2014 | 1.3     | Rewrite the key date and cross shipping information.<br>Add FAQ (XTP343) for additional documentation. |

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